

REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is requested. Claims 65-80 are in this application. Claims 1-64 have been cancelled. Claims 65-80 have been added to alternately claim the present invention.

New claim 65 recites, in part:

"A method of forming a conductor on a semiconductor structure, the semiconductor structure having a layer of insulation material and a via that contacts the layer of insulation material, the layer of insulation material having a top surface, the method comprising:

"etching the top surface of the layer of insulation material to form a plurality of spaced-apart first openings in the top surface of the layer of insulation material, each first opening having a bottom surface that lies below the top surface of the layer of insulation material; and

"simultaneously etching the top surface of the layer of insulation material and the bottom surface of each first opening to form a second opening in the top surface of the layer of insulation material, and lower the bottom surface of each first opening to form a plurality of spaced-apart lowered first openings that expose the via, the second opening having a top that lies in a common plane with the top surface of the layer of insulation material and includes no portion of the top surface of the layer of insulation material, and a bottom that lies below the top surface of the layer of insulation material, each of the plurality of spaced-apart lowered first openings extending away from the bottom of the second opening."

With respect to Tseng (U.S. Patent No. 5,741,741), this reference first teaches in FIG. 1 the formation of an insulating layer 16, which is followed by the formation of a hard mask 18. The Tseng reference next teaches in FIGS. 2-3 that a number of trenches 13 are formed in insulating layer 16. To form the trenches, a layer of photoresist 20 is formed on hard mask 18, and then patterned.

Next, the hard mask 18 is etched. Following this, insulating layer 16 is etched to form the trenches 13. (See also column 5, line 14 to column 6, line 21 of Tseng.)

It is assumed that the Examiner would read the formation of trenches 13 to constitute the "etching the top surface . . . to form a plurality of spaced-apart first openings" element required by claim 65.

In FIGS. 4-7, the Tseng reference next teaches that a number of via/plug openings are etched in the bottom surfaces of the trenches 13 to expose select regions on the top surfaces of the conducting traces 14. To form the via/plug openings, patterned resist layer 20 is laterally etched to form patterned resist layer 20' which, in turn, exposes more of the hard mask 18. The newly exposed regions of hard mask 18 are then etched. (See FIGS. 4 and 5, and column 6, lines 33-50 of Tseng.)

Following this, resist layer 20' is removed, and replaced by a patterned resist layer 24. As taught by Tseng, patterned resist layer 24 has "openings over the trenches 13' where the T-shaped metal plug contact openings are to be formed while masking from etching the remaining portions of the trenches." (See FIG. 6 and column 6, lines 53-57 of Tseng.)

After this, as shown in FIG. 7 of Tseng, the exposed regions of the top surface of insulating layer 16, along with the exposed regions of the bottom surfaces of the trenches 13, are etched to form a left-side plug contact opening 17 and a right-side plug contact opening 17, which expose the surface of the first level of interconnections 14. (See from column 6, lines 66 to column 7, lines 3 of Tseng.)

The FIG. 7 etch step, however, can not be read to constitute the "simultaneously etching" element required by claim 65. As noted above, the "simultaneously etching" element forms a second opening in the top surface of the layer of insulation material, and lowers the bottom surface of each first opening to form a plurality of spaced-apart lowered first openings.

In addition, each of the plurality of spaced-apart lowered first openings must extend away from the bottom of the second opening. However, although the FIG. 7 etch lowers portions of the bottom surfaces of the trenches 13, the Tseng reference

fails to teach or suggest that each of the lowered portions of the trenches 13 extends away from an opening which can be read to be the second opening required by claim 65.

For example, although the lower section of the left-side plug contact opening 17 shown in FIG. 7 of Tseng extends away from an upper wider section of the left-side plug contact opening 17 following the FIG. 7 etch, the upper wider section of the left-side plug contact opening 17 can not be read to be the second opening required by claim 65. This is because the other lower sections (e.g., of the right-side plug contact opening 17) do not also extend away from the upper wider section of the left-side plug contact opening 17.

Thus, since the Tseng reference fails to teach or suggest that each of the lowered portions of the trenches 13 extends away from an opening which can be read to be the second opening, claim 65 is patentable over the Tseng reference. In addition, claims 66-68 depend either directly or indirectly from claim 65, and are therefore patentable over the Tseng reference for the same reasons as claim 65.

With respect to Chittipeddi (U.S. Patent No. 6,417,087), this reference first teaches in FIGS. 4A-4D the formation of a lower dielectric film 11, a barrier layer film 13, and an upper dielectric film 15. Next, as shown in FIG. 4E, Chittipeddi teaches the formation and patterning of a mask 31, followed by an etch through upper dielectric film 15 that forms bond pad opening 20. After this, as shown in FIGS. 4F and 4G, Chittipeddi teaches the formation and patterning of a mask 33, followed by an etch through lower dielectric film 11 that forms via openings 19 that expose the top surface 6 of conductive film 5.

The Chittipeddi reference also teaches that the masking and etch steps in FIGS. 4E and 4F can be reversed such that the via openings are first formed through upper dielectric film 15. After this, upper dielectric film 15 is etched to form bond pad opening 20 which, at the same time, etches through lower dielectric film 11 to

lower the bottom surfaces of the via openings to expose the top surface 6 of conductive film 5. (See from column 6, line 54 to column 7, line 4 of Chittipeddi.)

Although the Chittipeddi reference teaches simultaneously etching through the upper dielectric film 15 and the lower dielectric film 11 to form bond pad opening 20, and lower the bottom surfaces of the via openings to expose the top surface 6 of metal trace 5, this step can not be read to constitute the “simultaneously etching” element required by claim 65. This is because Chittipeddi fails to teach or suggest that the lowered bottom surfaces of the via openings 19 expose another via. Instead, as shown in 4G, the Chittipeddi reference teaches that the lowered bottom surfaces of the via openings 19 expose the top surface 6 of conductive film 5.

Thus, since the Chittipeddi reference fails to teach or suggest that the via openings expose another via, claim 65 is patentable over the Chittipeddi reference. In addition, claims 66-68 depend either directly or indirectly from claim 65, and are therefore patentable over the Chittipeddi reference for the same reasons as claim 65.

In addition, from what can be determined, the Adams reference (U.S. Patent No. 6,566,242), the Yu reference (U.S. Patent No. 5,952,704), and the Inohara reference (U.S. Patent No. 5,976,972) do not teach or suggest forming via openings which have bottom surfaces that expose another via. As a result, claims 65-68 are patentable over Adams, Yu, and Inohara.

New claim 69 recites, in part:

"A method of forming a conductor on a semiconductor structure, the semiconductor structure having a layer of insulation material and a contact that touches the layer of insulation material, the layer of insulation material having a top surface, the method comprising:

"etching the top surface of the layer of insulation material to form a plurality of spaced-apart first openings in the top surface of the layer of insulation material, each first opening having a bottom surface that lies below the top surface of the layer of insulation material; and

"simultaneously etching the top surface of the layer of insulation material and the bottom surface of each first opening to form a second opening in the top surface of the layer of insulation material, and lower the bottom surface of each first opening to form a plurality of spaced-apart lowered first openings that expose the contact, the second opening having a top that lies in a common plane with the top surface of the layer of insulation material and includes no portion of the top surface of the layer of insulation material, and a bottom that lies below the top surface of the layer of insulation material, each of the plurality of spaced-apart lowered first openings extending away from the bottom of the second opening."

New claim 69 differs from new claim 65 in that new claim 69 recites a contact in lieu of a via. Thus, with respect to Tseng, each of the comments made with respect to claim 65 also apply to new claim 69 (i.e., the Tseng reference fails to teach or suggest in FIG. 7 that each of the lowered portions of the trenches 13 extends away from an opening which can be read to be the second opening). As a result, claim 69 is patentable over the Tseng reference. In addition, claims 70-72 depend either directly or indirectly from claim 69, and are therefore patentable over the Tseng reference for the same reasons as claim 69.

With respect to Chittipeddi, FIG. 4G of this reference also fails to teach or suggest that the lowered bottom surfaces of the via openings 19 expose the top surface of a contact. Thus, since the Chittipeddi reference fails to teach or suggest that the via openings 19 expose a contact, claim 69 is patentable over the Chittipeddi reference. In addition, claims 70-72 depend either directly or indirectly

from claim 69, and are therefore patentable over the Chittipeddi reference for the same reasons as claim 69.

In addition, from can be determined, the Adams reference, the Yu reference, and the Inohrara reference do not teach or suggest forming via openings which have bottom surfaces that expose a contact. As a result, claims 69-72 are patentable over Adams, Yu, and Inohara.

New claim 73 recites, in part:

“A method of forming a conductive line on a semiconductor structure, the semiconductor structure having a layer of insulation material, the layer of insulation material having a top surface, the method comprising:

“etching the top surface of the layer of insulation material to form a plurality of spaced-apart first trenches in the top surface of the layer of insulation material, each first trench having a bottom surface that lies below the top surface of the layer of insulation material, a first width, and a first length that is substantially greater than the first width; and

“simultaneously etching the top surface of the layer of insulation material and the bottom surface of each first trench to form a second trench in the top surface of the layer of insulation material, and lower the bottom surface of each first trench to form a plurality of spaced-apart lowered first trenches, the second trench having a top that lies in a common plane with the top surface of the layer of insulation material and includes no portion of the top surface of the layer of insulation material, a bottom that lies below the top surface of the layer of insulation material, a second width, and a second length that is substantially greater than the second width, each of the plurality of spaced-apart lowered first trenches extending away from the bottom of the second trench and having a third width and a third length that is substantially greater than the third width.”

As discussed above, the Tseng reference fails to teach or suggest in FIG. 7 that each of the lowered portions of the trenches 13 extends away from an opening which can be read to be the second opening. Similarly, the Tseng reference fails to teach or suggest in FIG. 7 that each of the lowered portions of the trenches 13 extends away from a trench which can be read to be the second trench. As a result, claim 73 is patentable over the Tseng reference. In addition, claims 74-80 depend

either directly or indirectly from claim 73, and are therefore patentable over the Tseng reference for the same reasons as claim 73.

With respect to Chittipeddi, although this reference teaches simultaneously etching through the upper dielectric film 15 and the lower dielectric film 11 to form bond pad opening 20, and lower the bottom surfaces of the via openings 19 to expose the top surface 6 of metal trace 5, this step can not be read to constitute the "simultaneously etching" element required by claim 73. This is because Chittipeddi fails to teach or suggest that the bond pad opening 20 is formed as a trench that has a width and a length that is substantially greater than the width. Instead, as shown in FIG. 3, Chittipeddi teaches that the bond pad opening is square.

Thus, since the Chittipeddi reference fails to teach or suggest that the bond pad opening 20 is formed as a trench which has a length that is substantially greater than a width, claim 73 is patentable over the Chittipeddi reference. In addition, claims 74-80 depend either directly or indirectly from claim 73, and are therefore patentable over the Chittipeddi reference for the same reasons as claim 73.

In addition, from can be determined, the Adams reference, the Yu reference, and the Inohrara reference do not teach or suggest forming bond pad openings with lengths that are substantially greater than the widths. As a result, claims 73-80 are patentable over Adams, Yu, and Inohara.

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Thus, for the foregoing reasons, it is submitted that the application is in a condition for allowance. Therefore, the Examiner's early re-examination and reconsideration are respectively requested.

Respectfully submitted,

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